Description

EMBEDDED EEPROM CELL AND METHOD OF FORMING THE SAME

Technical Field

The present invention relates generally to the non-volatile memory devices and more particularly to a non-volatile memory embedded logic device.

Background Art

Non-volatile memory cells such as EEPROM cells typically have a double-layer polycrystalline silicon ("poly") structure that includes a control gate layer and a floating gate layer. In contrast, semiconductor logic gates, having a control gate only, require only a single polysilicon process to form the control gate layer. To improve computing speed and reduce device size, non-volatile memory cells are sometimes embedded into logic chips. Since processes for forming a non-volatile memory cell and a logic gate are quite different, they are traditionally formed in a separate series of steps.

To reduce a total number of processing steps for a non-volatile memory embedded logic circuit, it is often desirable to form the embedded non-volatile memory cells using a single-layer poly structure. Figure 1A shows a cross-section of a typical single-layered EEPROM cell 10 dissected along a wordline. Figure 1B shows a cross-section of the same EEPROM cell 10 dissected along a bitline. With reference to Figure 1A, a P-channel single poly EEPROM cell 10 is formed in an N-well 14 provided within a P-substrate. With reference to Figure 1B, the EEPROM cell 10 includes a P-channel select transistor 24 and a P channel storage transistor 26. A first P+ diffusion region 28 serves as both a drain for storage transistor 26 and a source for select transistor

24, and a second P+ diffusion region 30, which is coupled to a bitline 36, serves as a drain for select transistor 24. The single-layer polysilicon 20 serves as a floating gate for the storage transistor 26 and a select gate for the select transistor 24. Referring back to Figure 1A, an application of a bias voltage to a control gate 12 enhances a channel 22 (Figure 1B) extending between a source 32 and the drain 28 of storage transistor 26, and an application of a bias voltage to the select gate 24 enhances a channel 34 between the source 28 and the drain 30 of select transistor 24.

Referring again to Figure 1A, a P-type buried diffusion layer serves as the control gate 12 for the EEPROM cell 10. A layer of silicon oxide 18 that is approximately 350 Å thick is provided between the floating gate 20 and the control gate 12. A tunnel oxide layer 16 that is about 70 Å thick lies between the floating gate 20 and the N-well 14. The single-poly silicon EEPROM cell 10 is programmed, erased, and read in a manner similar to that of a double-poly silicon cell. That is, programming is accomplished by electron tunneling from the floating gate 20 to the substrate 14 through the tunnel oxide 16 while erasing is realized by electrons tunneling from the substrate 14 to the floating gate 20.

Although the single poly silicon process described above allows the formation of a single polysilicon layer for both the floating gates of non-volatile memory cells and the control gates of the logic cells in the same step, the oxide layer underneath the polysilicon layer has to be formed in separate steps because its thickness varies throughout the embedded circuit. For instance, the thickness of a typical gate oxide layer for a low voltage logic gate is approximately 130 Å for 5V systems, 50 Å for 2.5V systems and 30 Å for 1.8V systems. On the other hand, the tunnel oxide layer

and the oxide layer between the floating gate and the control gate of a EEPROM cell is typically around 70 Å thick. Because the oxide layer thickness of the logic cells and the EEPROM cells are so different, they are typically formed in separate steps. For instance, U.S. Patent No. 6,238,979 to Bergemont teaches an embedment of EEPROM cells in a logic device by forming the EEPROM cells first, followed by masking the completed EEPROM cells to form logic gates. It would be desirable to have an embedded circuit structure and a method for forming the structure that would allow the formation of the oxide layer for both the logic gate and the non-volatile memory cell in one step, thereby eliminating the need to form the EEPROM cells and the logic gates separately.

Disclosure of the Invention

The present invention teaches the formation of a non-volatile memory embedded logic circuit having three types of active areas: one for the non-volatile memory cells, one for low voltage logic gates, and one for high voltage logic gates. The low voltage logic gate and the non-volatile memory cell having an oxide layer of essentially the same thickness while the high voltage logic gate has an oxide layer that is thicker. The embedded memory structure disclosed herein allows the forming of the non-volatile memory gate oxide layer and the logic gate oxide layer in a single step, thereby reducing manufacturing time.

Brief Description of the Drawings

Figure 1A shows a cross section of a prior art single-polysilicon non-volatile memory dissected along a wordline.

Figure 1B shows a cross section of the prior art single-polysilicon non-volatile memory dissected along a bit line.

Figure 2A shows a top view of a single-polysilicon EEPROM cell according to one exemplary embodiment of the present invention.

Figure 2B shows a cross-sectional view of the single-polysilicon EEPROM cell shown in Figure 2A taken along line A-A.

Figure 2C shows a cross-sectional view of the single-polysilicon EEPROM cell shown in Figure 2A taken along line B-B, a cross-sectional view of a low voltage logic gate cell, and a high voltage logic gate cell of the present invention.

Figure 3A shows the step-by-step formation of a low voltage logic gate and a high voltage logic gate according to the preferred embodiment of the present invention.

Figure 3B shows the step-by-step formation of a single-polysilicon non-volatile memory cell according to the preferred embodiment of the present invention.

Modes for Carrying Out the Invention

In Figure 2A, a top view of an EEPROM cell 100 according to an exemplary embodiment of the present invention is shown. A cross-sectional view of the EEPROM cell 100 taken along the wordline (segmenting line A-A) is shown in Figure 2B. A cross-sectional view of the EEPROM cell 100 taken along the bitline (segmenting line B-B) is shown alongside a high voltage logic gate 96 and a low voltage logic gate 94 in Figure 2C.

With reference to Figures 2A-2C, the EEPROM cell 100 is made up of a buried control gate 80, a floating gate 82, and a tunneling region 84 comprised of a tunneling extension 86 below the floating gate 82. The control gate 80 is connected to a voltage source through a tungsten plug 88. There are basically two oxide layers throughout the whole embedded circuit: a thick oxide layer 90 for the high voltage logic gate 96 and the

select gate 98, and a thinner oxide layer 92 for a tunnel oxide of the EEPROM cell 100 and the low voltage logic gate 94.

Exemplary process steps for simultaneously forming the EEPROM cell 100 and the logic gates 94, 96, 98 are shown in Figures 3A and 3B. Figure 3A shows the steps for making a high voltage MOS transistor and a low voltage MOS transistor. Figure 3B shows the steps for making an EEPROM cell as seen in a cross-sectional view taken along a wordline. Although not shown in the figures for purposes of brevity and clarity, it will be understood that various other processing steps may be performed in between the steps shown. These steps may include, for example, ion implantation steps to form various N-well and P-well regions and the formation of tungsten plugs to the control gates.

In step (i), a pad oxide layer 44 is formed on top of a semiconductor substrate 46 followed by a deposition of a nitride layer 42 on top of the pad oxide layer 44. Next, a photoresist layer 40 is formed on top of the nitride layer 42, patterned and etched, so as to expose an area 50 where an isolation structure is to be formed. The isolation structure surrounds and electrically isolates individual device regions in which logic cells and embedded memory cells are built. Though the isolation structure shown in subsequent figures are of the Shallow Trench Isolation (STI) type, it is also possible to use other isolation methods such as Local Oxidation of Silicon (LOCOS). In an STI process, the isolation structure is formed by etching a shallow trench through the pad oxide 44 and nitride layer 42 and into an exposed substrate area to a depth of about 4000 Å and then filled with, for example, a silicon oxide using a deposition process according to methods known to one skilled in the art. As shown in step (ii), a shallow trench 48 is formed by an etch of the exposed area 50

followed by an oxide fill step that fills the shallow trench with silicon oxide. Using the nitride layer 42 as a natural stop, a subsequent planarization process, such as a chemical mechanical planarization (CMP) process, polishes off any excess silicon oxide material, forming a leveled oxide plateau 49 on top of the STI structure 48.

The nitride layer 42 and the pad oxide layer 44 are then sequentially removed to form an STI isolation structure 48 shown in step (iii). An N+ doping region is implanted in the EEPROM cell area to form the control gate 80 (shown in Figure 2B). Next, as shown in step (iv), a high voltage (HV) gate oxide layer 68 of approximately 250 Å thickness is formed on top of the substrate 46. Subsequently, the oxide layer 68 is masked with a photoresist that is patterned to define areas 52, 54 where a thinner oxide layer is to be formed. The formation of the oxide may be carried out by thermal oxidation of the substrate, chemical vapor deposition, or atomic layer deposition. The exposed part of the oxide layer 68 is then etched to reveal the underlying substrate 46 as shown in step (v). In step (vi), a thin oxide layer 56, 58 approximately 70 Å thick is formed on the exposed substrate 46. This layer of thin gate oxide 56, 58 serves as a gate oxide 56 for the low voltage (LV) logic gate and a tunnel oxide 58 for the EEPROM cell respectively. Thereafter, as shown in Figure (vii), a polysilicon layer 64, 66 is deposited on top of the oxide layer 68 to form a control gate 64 in the logic gate area and a floating gate 66 in the EEPROM cell area respectively.

Although the present invention has been described in terms of specific exemplary embodiments, one skilled in the art will realize that other embodiments may be readily envisioned that are still the present invention. Therefore, the present invention shall be limited in scope only by the appended claims.